

ABSTRACT

A circuit arrangement for generating non-overlapping clock phases including a first circuit, a second circuit, and a multiplexer. The first circuit combines two input signals to form an output signal, and a first input provides for application of a common clock signal. The second circuit combines two input signals to form an output signal, and a first input provides for application of the common clock signal. The multiplexer has a first input connected to an output of the first circuit, a second input connected to an output of the second circuit, and an output connected to a second input of each of the first and second circuits, and has a third input that switches between the first and second inputs of the multiplexer for application of the clock signal. A plurality of non-overlapping clock phases are provided by output signals of the first and second circuits and of the multiplexer.